What is claimed is:

1. A method of fabricating a piezoelectric film having a patterned electrode deposited on a substrate, the electrode having an edge with a height, comprising the step of reducing or eliminating the height of the edge, wherein a weakening effect at the edge is diminished.

2. The method of claim 1, wherein the piezoelectric film is selected from the group consisting of:

a) aluminum nitride; and

b) zinc oxide.

3. The method of claim 1, wherein the patterned electrode is selected from the group consisting of aluminum and titanium.

4. The method of claim 1 wherein the substrate is selected from the group consisting of silicon and gallium arsenide.

5. The method of claim 1, wherein the step of reducing or eliminating the height of the edge comprises the substeps of:

a) depositing a non-conducting layer on the patterned electrode and the substrate; and

b) planarizing the non-conducting layer such that the non-conducting layer is of a same height as the patterned electrode.

6. The method of claim 5, wherein substep (b) is achieved using chemical mechanical polishing.

7. The method of claim 5, wherein substep (b) is achieved using polymer planarization.

8. The method of claim 5, wherein step (b) is achieved using reflow and lift-off.

9. The method of claim 5, wherein the non-conducting layer has a low dielectric constant.

10. The method of claim 5, wherein the non-conducting layer is SiO_2.

11. The method of claim 1, wherein the step of reducing or eliminating the height of the edge results in a stair-step shaped electrode.

12. The method of claim 11, wherein the step of reducing or eliminating the height of the edge comprises the substeps of:

a) depositing a plurality of conducting layers on the substrate wherein alternate layers are composed of a first conducting material and adjacent layers are composed of a conducting material which is different from the first conducting material such that adjacent layers have a different etch profile from each other;

b) selectively laterally etching a first conducting layer;

c) selectively laterally etching a second conducting layer directly below said first conducting layer; and

d) stopping step (c) at a point where said second conducting layer is etched less than said first conducting layer; and

e) repeating steps (b) through (d) for any additional conducting layers;

such that a stair-step electrode is formed.

13. The method of claim 12, wherein said alternating conducting layers are composed of titanium and aluminum.

14. The method of claim 1, wherein the step of reducing or eliminating the height of the edge results in a dome-shaped electrode.

15. The method of claim 14, wherein the step of reducing or eliminating the height of the edge comprises the substeps of:

a) depositing a resist layer on an electrode layer;

b) shaping said resist layer into a dome-shaped drop; and

c) etching the resist layer and the electrode layer until said electrode layer is shaped like a dome.

16. The method of claim 1, wherein the step of reducing or eliminating the height of the edge comprises the substeps of:

a) depositing a non-conducting layer on the substrate;

b) patterning the non-conducting layer such that a pattern of said non-conducting material is identical to a pattern desired for the electrode;

c) depositing a plurality of layers on said non-conducting layer;

d) depositing a masking film on a backside of the substrate;

e) patterning the masking film;

f) etching the backside of the substrate until the non-conducting layer is reached; and

g) etching a portion of the conducting layers which are not masked by the non-conducting layer.

17. The method of claim 16, wherein the non-conducting layer has a low dielectric constant.

18. The method of claim 16, wherein the non-conducting layer is SiO_2.